**DAILY ASSESSMENT FORMAT**

|  |  |  |  |
| --- | --- | --- | --- |
| **Date:** | **6/5/20** | **Name:** | **Sathya br** |
| **Course:** | **DIGITAL DESIGN USING HDL** | **USN:** | **4al16ec065** |
| **Topic:** | Verilog Tutorials and practice programs  Building/ Demo projects using FPGA | **Semester & Section:** | **6th semister**  **B section** |
| **Github Repository:** | **sathyabr** |  |  |

|  |
| --- |
| **FORENOON SESSION DETAILS** |
| **Image of session**  . |
| **Report**  **Verilog is a Hardware Description Language; a textual format for describing electronic circuits and systems. Applied to electronic design, Verilog is intended to be used for verification through simulation, for timing analysis, for test analysis (testability analysis and fault grading) and for logic synthesis.The Verilog HDL is an IEEE standard - number 1364. The first version of the IEEE standard for Verilog was published in 1995. A revised version was published in 2001; this is the version used by most Verilog users. The IEEE Verilog standard document is known as the Language Reference Manual, or LRM. This is the complete authoritative definition of the Verilog HDL.A further revision of the Verilog standard was published in 2005, though it has little extra compared to the 2001 standard. SystemVerilog is a huge set of extensions to Verilog, and was first published as an IEEE standard in 2005. See the appropriate Knowhow section for more details about SystemVerilog.IEEE Std 1364 also defines the Programming Language Interface, or PLI. This is a collection of software routines which permit a bidirectional interface between Verilog and other languages (usually C).Note that VHDL is not an abbreviation for Verilog HDL - Verilog and VHDL are two different HDLs. They have more similarities than differences, however.The history of the Verilog HDL goes back to the 1980s, when a company called Gateway Design Automation developed a logic simulator, Verilog-XL, and with it a hardware description language.Cadence Design Systems acquired Gateway in 1989, and with it the rights to the language and the simulator. In 1990, Cadence put the language (but not the simulator) into the public domain, with the intention that it should become a standard, non-proprietary language.The Verilog HDL is now maintained by a non profit making organisation, Accellera, which was formed from the merger of Open Verilog International (OVI) and VHDL International. OVI had the task of taking the language through the IEEE standardisation procedure.In December 1995 Verilog HDL became IEEE Std.**  **FPGAFPGA Basics – A Look Under the Hood An introductory look inside Field Programmable Gate Arrays. We’ll go over:Strengths & Weaknesses of FPGAs How FPGAs work What’s inside an FPGA So you keep hearing about FPGAs being utilized in more and more applications, but aren’t sure whether it makes sense to switch to a new technology. Or maybe you’re just getting into the embedded world and want to figure out if an FPGA-based system makes sense for you or not.This paper provides an overview of some of the key elements of FPGAs for engineers interested in utilizing FPGA-based technologies. It’s worth noting that this is a complex topic, and as such, some topics are not covered, some are just introductory, and others will evolve over time. This paper should still give you a lot of helpful information if you’re new to the world of FPGAs.What are the most important things you should know right away?Get out of the software mindset – You’re not writing software. Let me say that again because this is the single most important point if you’re thinking about working with FPGAs.You-are-NOT-writingsoftware.You’re designing a digital circuit. You’re using code to tell the chip how to configure itself.Plan for lots of bugs – yes, plan for them. They are going to happen. Way more than you expected. If you’re a newbie developer, you need to pull in someone that has experience with FPGA development to help with this estimate.Application-specific realities – you ought to concern yourself with realities revolving around cyber security and safety, as FPGAs are a different animal than what you’re likely used to.What is an FPGA?An FPGA is a (mostly) digital, (re-)configurable ASIC. I say mostly because there are analog and mixed-signal aspects to modern FPGAs. For example, some have A/D converters and PLLs. I put re- in parenthesis because there are actually one-timeprogrammable FPGAs, where once you configure them, that’s it, never again. However, most FPGAs you’ll come across are going to be re-configurable. So what do I mean by digitally configurable ASIC?I mean that at the core of it, you’re designing a digital logic circuit, as in AND, OR, NOT, flip-flops, etc. Of course that’s not entirely accurate and there’s much more to it than that, but that is the gist at its core.he players –There are currently two big boys: Altera (part of Intel) and Xilinx, and some supporting players (e.g. Actel (owned by Microsemi)).**  T-FLIP FLOP  module tff (t,clk,q,qb);  input t,clk;  output q,qb;  reg q, qb;  initial  begin  q=0;  q=1;  end  always@(posedge (clk))  begin  if(t==0) q=q;  else  q=qb;  qb=~q;  end  endmodule |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Date:** | **6/5/20** | **Name:** | **Sathya br** | |
| **Course:** | **Python Core and Advanced** | **USN:** | **4al16ec065** | |
| **Topic:** | **List Comprehensions** | **Semester & Section:** | **6th semister**  **B section** | |
| **AFTERNOON SESSION DETAILS** | | | |
| **Image of session** | | | |
| **Report**   * **List Comprehensions** * **Cube of numbers in a list** * **Even numbers in a list** * **Product of numbers in a list** * **Common elements in a list** | | | |